L Number	Hits	Search Text	DB	Time stamp
1	7620	((438/780) or (438/781) or (438/782) or (438/692) or (438/626) or (438/631) or (438/633) or (438/693) or (438/725) or (438/697) or (438/699) or (438/760)).CCLS.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/05 13:57
2	39447	cmp or (chemical adj mechanical adj (polishing or planarizing))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/05 13:58
3	421221	resist or photoresist	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/05 13:59
5	19	(((438/780) or (438/781) or (438/782) or (438/692) or (438/626) or (438/631) or (438/633) or (438/693) or (438/725) or (438/697) or (438/699) or (438/760)).CCLS.) and ((cmp or (chemical adj mechanical adj (polishing or planarizing))) near (resist or photoresist))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/05 13:59
4	157	(cmp or (chemical adj mechanical adj (polishing or planarizing))) near (resist or photoresist)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/05 14:25
6	1420928	remove	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/05 14:25
7	8268	remove near (resist or photoresist)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/05 14:25
8	17	(remove near (resist or photoresist)) with (cmp or (chemical adj mechanical adj (polishing or planarizing)))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/05 14:25
-	1	("0000424").PN.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/05/28 13:47
-	49798	trench	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/05/28 13:47
-	389	trench and shore	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/05/28 13:48
-	4	(trench and shore) and (sti or (shallow adj trench adj isolation))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/05/28 14:29
-	1055	(438/692).CCLS.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/11/25 12:44

-	14	((438/692).CCLS.) and (shore or (shore adj D))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/05/28 14:35
-	3	(((438/692).CCLS.) and (shore or (shore adj D))) and (sti or (shallow adj trench adj isolation))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/05/28 14:35
-	114633	(silicon adj (substrate or wafer))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/05/28 15:34
-	127	((silicon adj (substrate or wafer))) and (shore or (shore adj d))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/05/28 15:49
-	4	(((silicon adj (substrate or wafer))) and (shore or (shore adj d))) and trench	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/05/28 15:49
-	1	("20020160546").PN.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/11/25 13:07
-	14734	photo adj resist	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/11/25 13:15
-	3895	trench adj fill$2	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/11/25 13:09
-	53493	trench	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/11/25 13:09
-	22142	cmp	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/11/25 13:10
-	23096	planariz$3	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/11/25 13:10
-	138	(photo adj resist) and (trench adj fill$2)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/11/25 13:10
-	61	((photo adj resist) and (trench adj fill$2)) and cmp	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/11/25 13:10
-	47	(((photo adj resist) and (trench adj fill$2)) and cmp) and planariz$3	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/11/25 13:10

-	266601	resist	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/11/25 13:15
-	14734	(photo adj resist) and resist	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/11/25 13:16
-	856	(trench adj fill$2) and resist	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/11/25 13:16
-	351	cmp and ((trench adj fill$2) and resist)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/11/25 13:16
-	254	(cmp and ((trench adj fill$2) and resist)) and planariz$3	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/11/25 13:17
-	2	("5173439" | "5719073").PN.	USPAT	2002/11/25 13:39
-	1	6107187.URPN.	USPAT	2002/11/25 13:39
-	2969	((438/780) or (438/781) or (438/782) or (438/692) or (438/633)).CCLS.	USPAT; US-PGPUB	2003/11/05 13:53
-	200436	resist or (photo near2 resist)	USPAT; US-PGPUB	2003/07/09 13:35
-	838	(((438/780) or (438/781) or (438/782) or (438/692) or (438/633)).CCLS.) and (resist or (photo near2 resist))	USPAT; US-PGPUB	2003/07/09 13:34
-	24655	((resist or (photo near2 resist)) near (layer or film))	USPAT; US-PGPUB	2003/07/09 13:35
-	354	(((resist or (photo near2 resist)) near (layer or film))) and (((438/780) or (438/781) or (438/782) or (438/692) or (438/633)).CCLS.)	USPAT; US-PGPUB	2003/07/09 14:46
-	1	6117798.URPN.	USPAT	2003/07/09 14:38
-	6	("5607880" | "5747381" | "5783482" | "5948700" | "6030706" | "6030892").PN.	USPAT	2003/07/09 14:38
-	1373	((438/424) or (438/427) or (438/443)).CCLS.	USPAT; US-PGPUB	2003/07/09 14:46
-	23154	(cmp or ((chemical adj mechanical) near2 polish))	USPAT; US-PGPUB	2003/10/23 16:31
-	717	(((438/424) or (438/427) or (438/443)).CCLS.) and ((cmp or ((chemical adj mechanical) near2 polish)))	USPAT; US-PGPUB	2003/07/09 14:47
-	78	((((438/424) or (438/427) or (438/443)).CCLS.) and ((cmp or ((chemical adj mechanical) near2 polish)))) and (((resist or (photo near2 resist)) near (layer or film)))	USPAT; US-PGPUB	2003/07/09 15:59
-	71742	dish or dishing	USPAT; US-PGPUB	2003/07/09 15:59
-	443	(dish or dishing) and (((438/780) or (438/781) or (438/782) or (438/692) or (438/633)).CCLS.)	USPAT; US-PGPUB	2003/07/09 16:05
-	0	6436833.URPN.	USPAT	2003/07/09 16:28
-	6	("5173439" | "5721173" | "5880007" | "6001706" | "6048775" | "6107159").PN.	USPAT	2003/07/09 16:28
-	4	6171962.URPN.	USPAT	2003/07/09 16:45
-	5	("4613888" | "5094972" | "5298110" | "5702977" | "5817567").PN.	USPAT	2003/07/09 16:45
-	138	((((438/424) or (438/427) or (438/443)).CCLS.) and ((cmp or ((chemical adj mechanical) near2 polish)))) and (dish or dishing)	USPAT; US-PGPUB	2003/07/09 16:52

-	3875	((438/780) or (438/781) or (438/782) or (438/692) or (438/633)).CCLS.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/10/23 16:34
-	50475	(rie or (reactive near2 ion))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/10/23 16:30
-	32793	(cmp or ((chemical adj mechanical) near2 polish))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/10/23 17:10
-	1901	((rie or (reactive near2 ion))) same ((cmp or ((chemical adj mechanical) near2 polish)))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/10/23 16:31
-	156	(((438/780) or (438/781) or (438/782) or (438/692) or (438/633)).CCLS.) and (((rie or (reactive near2 ion))) same ((cmp or ((chemical adj mechanical) near2 polish))))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/10/23 16:31
-	7962	((438/780) or (438/781) or (438/782) or (438/692) or (438/633) or (438/693) or (438/697) or (438/698) or (438/699) or (438/700) or (438/702) or (438/703)).CCLS.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/10/23 16:37
-	12015	(photoresist or resist) and (cmp or (chemical adj mechanical adj planarize))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/10/23 17:11
-	1202	(((438/780) or (438/781) or (438/782) or (438/692) or (438/633) or (438/693) or (438/697) or (438/698) or (438/699) or (438/700) or (438/702) or (438/703)).CCLS.) and ((photoresist or resist) and (cmp or (chemical adj mechanical adj planarize)))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/10/23 16:48
-	129	((((438/780) or (438/781) or (438/782) or (438/692) or (438/633) or (438/693) or (438/697) or (438/698) or (438/699) or (438/700) or (438/702) or (438/703)).CCLS.) and ((photoresist or resist) and (cmp or (chemical adj mechanical adj planarize)))) and (((rie or (reactive near2 ion))) same ((cmp or ((chemical adj mechanical) near2 polish))))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/10/23 17:09
-	1377	(((rie or (reactive near2 ion))) same ((cmp or ((chemical adj mechanical) near2 polish)))) and ((photoresist or resist) and (cmp or (chemical adj mechanical adj planarize)))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/10/23 17:05
-	129	((((rie or (reactive near2 ion))) same ((cmp or ((chemical adj mechanical) near2 polish)))) and ((photoresist or resist) and (cmp or (chemical adj mechanical adj planarize)))) and (((438/780) or (438/781) or (438/782) or (438/692) or (438/633) or (438/693) or (438/697) or (438/698) or (438/699) or (438/700) or (438/702) or (438/703)).CCLS.)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/10/23 17:05
-	4048	((cmp or ((chemical adj mechanical) near2 polish))) same (photoresist or resist) and (cmp or (chemical adj mechanical adj planarize))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/10/23 17:11

-	4143	((cmp or ((chemical adj mechanical) near2 polish))) same (photoresist or resist)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/10/23 17:11
-	419832	(photoresist or resist)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/10/23 17:11
-	4143	((cmp or ((chemical adj mechanical) near2 polish))) same ((photoresist or resist))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/10/23 17:12
-	1296	((cmp or ((chemical adj mechanical) near2 polish))) with ((photoresist or resist))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/10/23 17:12
-	451	(((cmp or ((chemical adj mechanical) near2 polish))) with ((photoresist or resist))) and ((rie or (reactive near2 ion)))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/10/23 17:12
-	55	(((438/780) or (438/781) or (438/782) or (438/692) or (438/633) or (438/693) or (438/697) or (438/698) or (438/699) or (438/700) or (438/702) or (438/703)).CCLS.) and ((((cmp or ((chemical adj mechanical) near2 polish))) with ((photoresist or resist))) and ((rie or (reactive near2 ion))))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/10/23 17:15
-	624	(((rie or (reactive near2 ion))) same ((cmp or ((chemical adj mechanical) near2 polish)))) same ((photoresist or resist))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/10/23 17:17
-	42	((((rie or (reactive near2 ion))) same ((cmp or ((chemical adj mechanical) near2 polish)))) same ((photoresist or resist))) and (((438/780) or (438/781) or (438/782) or (438/692) or (438/633) or (438/693) or (438/697) or (438/698) or (438/699) or (438/700) or (438/702) or (438/703)).CCLS.)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/10/23 17:44
-	244	((cmp or ((chemical adj mechanical) near2 polish))) near2 ((photoresist or resist))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/10/23 17:44
-	28	(((cmp or ((chemical adj mechanical) near2 polish))) near2 ((photoresist or resist))) and (((438/780) or (438/781) or (438/782) or (438/692) or (438/633) or (438/693) or (438/697) or (438/698) or (438/699) or (438/700) or (438/702) or (438/703)).CCLS.)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/10/23 17:44
-	1	("6613690").PN.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/10/24 11:44
-	0	6613690.URPN.	USPAT	2003/10/24 11:44
-	8	("4385975" | "5065273" | "5077234" | "5100823" | "5723374" | "5759262" | "6130126" | "6420226").PN.	USPAT	2003/10/24 11:44
-	2	6420226.URPN.	USPAT	2003/10/24 11:54
-	9	("5468979" | "5805494" | "5972759" | "6013547" | "6080638" | "6130470" | "6150686" | "6174764" | "6340623").PN.	USPAT	2003/10/24 11:54

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

CLAIMS

[Claim(s)]
[Claim 1] An insulator layer with the level difference formed on the semiconductor substrate by the CMP method The process which forms an insulator layer all over the semiconductor substrate containing the effective element field in which it is the manufacture method of a semiconductor device including the process which carries out flattening, and the element composition member was formed, and the boundary region in which an element composition member is not formed, The process which forms a resist mask on the aforementioned insulator layer of the boundary region within predetermined distance from the aforementioned effective element field and the aforementioned effective element field, The manufacture method of the semiconductor device characterized by having the process which carries out specified quantity removal of the insulator layer exposed by the aforementioned boundary region by etching, the process which removes the aforementioned resist mask, and the process which carries out flattening of the aforementioned insulator layer by the CMP method.
[Claim 2] The aforementioned resist mask is the manufacture method of the semiconductor device according to claim 1 characterized by what is formed in the boundary region within the distance of 5 micrometers of abbreviation from the aforementioned effective element field and the aforementioned effective element field at least.
[Claim 3] The aforementioned resist mask is the manufacture method of the semiconductor device according to claim 1 or 2 further characterized by what is formed also in the predetermined field of the aforementioned boundary region by the predetermined pattern.
[Claim 4] The insulator layer exposed in the aforementioned circumference field in the process which carries out specified quantity removal of the insulator layer exposed in the aforementioned circumference field by etching is the manufacture method of the semiconductor device according to claim 1 characterized by what is considered as the abbreviation flat part of an insulator layer and the thickness of abbreviation same height which were formed in the aforementioned effective element field.
[Claim 5] The aforementioned element composition member is the manufacture method of a semiconductor device given in the claims 1, 2, and 3 or the 4th term characterized by what is been the wiring formed on the semiconductor substrate.
[Claim 6] The aforementioned element composition member is the manufacture method of a semiconductor device given in the claims 1, 2, and 3 or the 4th term characterized by what is been the active region which has the isolation structure formed on the semiconductor substrate.
[Claim 7] It is the manufacture method of the semiconductor device according to claim 6 characterized by what the aforementioned nitride functions as a stopper film of etching in the process which carries out specified quantity removal of the insulator layer which the nitride is formed on the semiconductor substrate which has the aforementioned isolation structure, and is exposed by the aforementioned boundary region by etching.
[Claim 8] It is the manufacture method of a semiconductor device given in the claims 1, 2, 3, 4, 5, and 6 or the 7th term characterized by what the aforementioned etching is performed for by the wet etching method in the process which carries out specified quantity removal of the insulator layer exposed by the aforementioned boundary region by etching.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[The technical field to which invention belongs] this invention relates to the manufacture method of the semiconductor device which includes in a detail the process which carries out flattening of the insulator layer with the level difference formed on the semiconductor substrate by the CMP method further about the manufacture method of a semiconductor device.
[0002]
[Description of the Prior Art] In the manufacture method of the semiconductor device in the former, when carrying out flattening of the oxide film in which the level difference is formed by the CMP method, changing a polish property sharply according to the level difference structure of a ground is known.
[0003] An example of the structure of the semiconductor substrate which does not form a dummy chip is explained to a boundary region based on drawing 5 . As shown in drawing 5 , the field (an effective element field is called hereafter) in which a semiconductor device is formed, and its boundary region are divided by the so-called grid line (G/L) field with a width of face of about 100 micrometers. The level difference with the insulator layer (for example, oxide film) of the same grade as a wiring level difference formed on the semiconductor substrate is formed. Moreover, since the circuit pattern is not formed in the boundary region, level difference density is 100% of abbreviation, and ****** after polish serves as the maximum. In addition, the marking field for checking a semiconductor substrate by looking is established in the boundary region.
[0004] For example, in a IMD/PMD(IMD/PMD:Inter Metal Dielectrics/Pre Metal Dielectrics)-CMP process, as shown in drawing 5 (b), the configuration of the wiring level difference of a ground and the insulator layer of an abbreviation same level difference are formed. Moreover, at a STI(STI:Shallow TrenchIsolation)-CMP process, as shown in drawing 5 (c), the insulator layer of the trench depth (nitride ****) and an abbreviation same level difference is formed.
[0005] At this time, the process which carries out flattening of the insulator layer is explained in an IMD/PMD-CMP process based on drawing 6 .
[0006] First, as shown in drawing 6 (a), the level difference structure of a boundary region 506 is a field which the oxide film 510 which circuit pattern density is 100% of abbreviation, and is an insulator layer has deposited most. Subsequently, as shown in drawing 6 (b), a slurry 512 is dropped, the polish pad 514 which is an elastic body is pushed, and barrel polishing of the oxide film 510 is carried out. At this time, the polish pad 514 deforms with a ground level difference, and the press force is locally unevenly distributed.
[0007] Then, since the polishing pressure force declines so that the circuit pattern density of a ground is high as shown in drawing 6 (c), polish speed becomes slow. That is, the polish speed of the boundary region (100% of circuit pattern density abbreviation) 506 in which wiring is not formed at all becomes slower than the polish speed of the effective element field in which wiring is formed (circuit pattern density is small), and the difference of the amount of polishes becomes remarkable. Subsequently, as shown in drawing 6 (d), even if the wiring level difference in an effective element field is lost, dispersion in ****** generated at the time of polish remains as it is. Moreover, since the structure of a boundary region 506 affects the structure of the effective element field 502, ****** of the G/L section 504 is finished thickly.
[0008] At the above-mentioned CMP process, since it is set up as criteria of the amount of polishes, if the abnormalities of ****** generate ****** of a normal effective device, it will also become the cause that an element is poor, for example by poor opening by defocusing of a pattern, or the etching stop at the time of etching.
[0009] Moreover, if a part of residual membrane in an effective element field is formed thickly, it will have a bad influence on a micro-processing process, and will also become the cause that the yield falls. Moreover, when dispersion in ****** occurs in an effective element field unlike the case where ****** of the whole effective element field becomes thick, there is a danger that wiring will be exposed in the effective element field center section, by carrying out superfluous polish.
[0010] The method of arranging the false device called a dummy element by the boundary region of an effective element field as a method of canceling such fault, and stabilizing the polish property of the periphery section is known.
[0011] An example of the structure of the semiconductor substrate in which the dummy element was formed is explained to a boundary region based on drawing 7 . As shown in drawing 7 , the field (an effective element field is called hereafter) in which a device element is formed, and its boundary region are divided by the so-called grid line (G/L) field with a width of face of about 100 micrometers. Moreover, the dummy element is arranged by the predetermined pattern at the boundary

region of an effective element field. The level difference with the insulator layer (oxide film) of the same grade as a wiring level difference formed on the semiconductor substrate is formed. Moreover, since the circuit pattern is formed in the boundary region, it is the same circuit pattern density as an effective element field. In addition, the marking field for checking a semiconductor substrate by looking is established in the boundary region. In addition, in this marking field, a dummy element is not arranged from the problem of visibility.
[0012] For example, in an IMD/PMD-CMP process, as shown in drawing 7 (b), the configuration of the wiring level difference of a ground and the insulator layer of an abbreviation same level difference are formed. Moreover, at a STI-CMP process, as shown in drawing 7 (c), the insulator layer of the trench depth (nitride ****) and an abbreviation same level difference is formed.
[0013] At this time, the process which carries out flattening of the insulator layer is explained in an IMD/PMD-CMP process based on drawing 8 .
[0014] First, as shown in drawing 8 (a), the level difference structure of a boundary region 606 is formed in the configuration of the dummy element 608 arranged to the boundary region 606, and is reduced to the same extent [actual circuit pattern density] as an effective element. Subsequently, as shown in drawing 8 (b), a slurry 612 is dropped, the polish pad 614 which is an elastic body is pushed, and barrel polishing of the oxide film 610 is carried out. At this time, the holding-down pressure force of the polish pad 614 becomes almost the same at the effective element field 602 and a boundary region 606.
[0015] then, the circuit pattern density in the boundary region 606 and effective element field where the dummy element 608 has been arranged as shown in drawing 8 (c) -- abbreviation -- since it is the same -- the polish speed in both fields -- abbreviation -- it becomes the same Furthermore, since the influence of a boundary region 606 is pressed down to the minimum when CMP polish is completed as shown in drawing 8 (d), the local abnormalities in thickness do not occur to the effective element field 602.
[0016] since this dummy element is formed in the boundary region of the same layer as an effective element field -- the circuit pattern density of a boundary region -- the circuit pattern density of an effective element field, and abbreviation -- it can form identically consequently, dispersion of polish speed -- small -- becoming -- an effective element field and a boundary region -- ****** -- abbreviation -- the same insulator layer is formed Moreover, at the end time of CMP polish, since the influence of a boundary region is suppressed, the abnormalities of local ****** do not occur in an effective element field.
[0017] Thus, since the polish property of an effective element field can be stabilized by arranging a dummy element to a circumference field, it is actually carried out as the manufacture method of a common semiconductor device.
[0018]
[Problem(s) to be Solved by the Invention] However, by the above-mentioned conventional method, there are the following problems, for example in the typical isolation (STI:Shallow Trench Isolation) CMP process which is a CMP adoption process, and the flattening (IMD/PMD:Inter Metal Dielectrics/Pre Metal Dielectrics) CMP process of the wiring level difference formed on the insulator layer.
[0019] (The 1st problem) Since it is necessary to perform patterning besides an effective element field in order to form a dummy element in a circumference field, the productivity (here, CoO (Cost Of Ownership) not only including a throughput but all production cost and man days is called productivity) in an exposure process falls remarkably. Moreover, although this patterning must be performed at all CMP processes, since it is not what contributes to productivity, there is a problem that mass-production nature gets worse.
[0020] (The 2nd problem) Although the marking field which carries out laser printing of the lot history (ID) exists in a circumference field again, in order to prevent visibility aggravation of a marking character, a dummy element is not arranged in this marking field. Thus, since the field in which a circuit pattern is not formed adjoins and exists in an effective element field, there is a problem that a polish property gets worse locally in a field in part.
[0021] Therefore, the purpose of this invention is in the thing which can acquire a suitable polish property and for which new and the improved manufacture method of a semiconductor device are offered in the flattening process by the CMP method, without reducing productivity.
[0022]
[Means for Solving the Problem] In order to solve the above-mentioned technical problem, in invention according to claim 1 An insulator layer with the level difference formed on the semiconductor substrate by the CMP method The process which forms an insulator layer all over a semiconductor substrate including the effective element field in which it is the manufacture method of a semiconductor device including the process which carries out flattening, and the element composition member was formed, and the circumference field in which an element composition member is not formed, The process which forms a resist mask on the aforementioned insulator layer of the circumference field within predetermined distance from the aforementioned effective element field and the aforementioned effective element field, The manufacture method of the semiconductor device characterized by having the process which carries out specified quantity removal of the insulator layer exposed in the aforementioned circumference field by etching, the process which removes the aforementioned resist mask, and the process which carries out flattening of the aforementioned insulator layer by the CMP method is offered.
[0023] In invention given in this paragraph, since the maldistribution of the pressure of the polish pad in a CMP process becomes small, the difference of polish speed is eased and the influence of ****** on the oxide film in an effective element field is avoided. Moreover, since it is not necessary to actually process a circuit pattern like the conventional dummy element, productivity improves. Furthermore, degradation of the visibility of a marking field is prevented before and after a polish

process and after the following process.
[0024] moreover, the aforementioned resist mask is formed in the circumference field within the distance of 5 micrometers of abbreviation from the aforementioned effective element field and the aforementioned effective element field at least like invention according to claim 2 -- it needs -- constituting is desirable At the oxide-film removal process (for example, wet etching process) which is the following process, it can consider as the design in consideration of the permeate lump of the medical fluid to a resist longitudinal direction.
[0025] moreover, the aforementioned resist mask is further formed also in the predetermined field of the aforementioned circumference field by the predetermined pattern like invention according to claim 3 -- it needs -- if constituted, since the level difference density of the oxide film of a circumference field will become of the same grade as the level difference density in an effective element field, the press force of a polish pad is also equalized Consequently, it is hard coming to generate the polish speed difference, and dispersion in residual membrane thickness is improved. Moreover, since it is not necessary to actually process a circuit pattern like the conventional dummy element, degradation of the visibility of a marking field is prevented before and after a polish process and after the following process.
[0026] In the process which carries out specified quantity removal of the insulator layer exposed in the aforementioned circumference field by etching like invention according to claim 4, moreover, the insulator layer exposed in the aforementioned circumference field it considers as the abbreviation flat part of an insulator layer and the thickness of abbreviation same height which were formed in the aforementioned effective element field -- it needs -- if constituted, since the level difference density of the oxide film of a circumference field will become of the same grade as the level difference density in an effective element field further, the press force of a polish pad is also equalized Consequently, further, it is hard coming to generate the polish speed difference, and dispersion in residual membrane thickness is improved.
[0027] moreover, the aforementioned element composition member is the wiring formed on the semiconductor substrate like invention according to claim 5 -- it needs -- if constituted, in case the level difference of the layer insulation film formed on wiring will be ground by the CMP method, a polish property improves
[0028] moreover, the aforementioned element composition member is an active region which has the isolation structure formed on the semiconductor substrate like invention according to claim 6 -- it needs -- if constituted, the polish property in the CMP flattening process of the oxide film in an isolation process will improve
[0029] moreover, on the semiconductor substrate which has the aforementioned isolation structure, the nitride is formed like invention according to claim 7, and the aforementioned nitride functions as a stopper film of etching in the process which carries out specified quantity removal of the insulator layer exposed in the aforementioned circumference field by etching -- it needs -- if constituted, in the process which removes an insulator layer, it is not necessary to carry out time control of the level difference formed strictly
[0030] moreover, in the process which carries out specified quantity removal of the insulator layer exposed by the aforementioned boundary region by etching like invention according to claim 8, the aforementioned etching is performed by the wet etching method -- it needs -- if constituted, an oxide film is removable by the cheap method
[0031]
[Embodiments of the Invention] Hereafter, the form of suitable operation of this invention is explained in detail, referring to an accompanying drawing. In addition, in the following explanation and an accompanying drawing, duplication explanation is omitted by ****** which attaches the same sign about the component which has the same function and same composition.
[0032] (Form of the 1st operation) The manufacture method of the semiconductor device concerning the form of the 1st operation is explained first, referring to drawing 1 . In addition, drawing 1 is cross-section process drawing for explaining the manufacture method of the semiconductor device concerning the form of the 1st operation. In addition, the IMD/PMD-CMP process is shown in this operation form.
[0033] First, as shown in drawing 1 (a), the insulator layer 110 which consists of an oxide film is formed on the semiconductor substrate 100 by which wiring 108 is formed in the effective element field 102. At this time, the dummy element is not arranged in the circumference field 106. The maximum level difference of an oxide film 110 crosses to this circumference field 106 broadly, and is formed in it.
[0034] This operation form or the fundamental wiring level difference structure of the semiconductor device to cut is the same as usual. Moreover, since a dummy element is not arranged to the circumference field 106, the circuit pattern density of the circumference field 106 is 100% of abbreviation, and the level difference of the oxide film 110 of the same grade as wiring height has generated it.
[0035] Subsequently, as shown in drawing 1 (b), the resist pattern 112 for masking 102 in an effective element field and the G/L field 104 is deposited on an oxide film 110 by package exposure. It is desirable to form the resist pattern 112 at this time 106, for example, a 5-micrometer circumference field. Since this is equal to the height of a wiring level difference as an amount of removal of an oxide film, it is the oxide-film removal process (for example, wet etching process) which is the following process, and is because a permeate lump of the medical fluid to a resist longitudinal direction is conjectured that about several micrometers occur. Therefore, it is necessary to carry out the OPA lap of about 5 micrometers of the resist patterns to a circumference field, and to form them.
[0036] Then, as shown in drawing 1 (c), specified quantity removal of the oxide film 110 exposed in the circumference field 106 is carried out by the wet etching method. namely, the level difference after removal of an oxide film 110 -- datum level (abbreviation flat side of an effective element field), and abbreviation -- it carries out by controlling etching time so that it

may become the same However, it is not necessary to perform a precise thickness control, and it is sufficient if it controls to the grade which wiring 108 does not expose. Therefore, since the need of the high controllability is not carried out but there are margins of enough also in a pattern size target, according to the wet etching method, a level difference is removable at an oxide-film removal process, as a cheap method.

[0037] Thus, since a circumference level difference is removed and polish is completed so that the oxide film 110 of the circumference field 106 may not be removed completely, in the polish process by the CMP method, the circuit pattern density of the circumference field 106 acts as 0% of abbreviation.

[0038] Finally, as shown in drawing 1 (d), after removing the resist pattern 112, an oxide film 110 is ground by the CMP method. this time -- a ground level difference -- level difference datum level -- receiving -- abbreviation -- since it is the same, the maldistribution of the press force of a polish pad becomes small Therefore, it is prevented that polish speed is delayed in an effective element field, without the polish speed difference occurring locally. Thus, since the polish speed of enough in an effective element field is in equilibrium, the influence which it has on ****** of an effective element field is small. Therefore, since the circumference field where the level difference was removed does not affect the circuit pattern of an effective element field, it can acquire a good polish property in an effective element field.

[0039] Although ground circuit pattern density is 100% of abbreviation, since this operation form **** has removed the level difference of a circumference field, it serves it as 0% of circuit pattern densities in a CMP process. Moreover, since an actual circuit pattern is not processed like the conventional dummy element, the visibility of a marking field is not worsened. Since the level difference of the pattern the non-formed field outside an effective element field is canceled before CMP polish, productivity improves conventionally. Moreover, since it can respond with a mask common to all layers, the increase in the number of masks can be suppressed. Also about a mask design rule and a winning-by-taking-two-half-points way, since the precision of about several micrometers is enough, there are few mask manufactures and increases in cost on an aspect of practical use, and they end.

[0040] (Form of the 2nd operation) In this operation form, in order to make the polish property of a circumference field approximate with the polish property of an effective element field as compared with the form of the 1st operation, a predetermined circuit pattern is formed in a circumference field.

[0041] First, the manufacture method of the semiconductor device concerning the form of the 2nd operation is explained, referring to drawing 2 . In addition, drawing 2 is cross-section process drawing for explaining the manufacture method of the semiconductor device concerning the form of the 2nd operation. In addition, the IMD/PMD-CMP process is shown in this operation form.

[0042] First, as shown in drawing 2 (a), the insulator layer 210 which consists of an oxide film is formed on the semiconductor substrate 200 by which wiring 208 is formed in the effective element field 202. At this time, the dummy element is not arranged in the circumference field 206. The maximum level difference of an oxide film 210 crosses to this circumference field 206 broadly, and is formed in it.

[0043] This operation form or the fundamental wiring level difference structure of the semiconductor device to cut is the same as usual. Moreover, since a dummy element is not arranged to the circumference field 206, the circuit pattern density of the circumference field 206 is 100% of abbreviation, and the level difference of the oxide film 210 of the same grade as wiring height has generated it.

[0044] Subsequently, as shown in drawing 2 (b), the resist pattern 212 for masking 202 in an effective element field and the G/L field 204 is deposited on an oxide film 210 by package exposure. It is desirable to form the resist pattern 212 at this time 206, for example, a 5-micrometer circumference field. Since this is equal to the height of a wiring level difference as an amount of removal of an oxide film, it is the oxide-film removal process (for example, wet etching process) which is the following process, and is because a permeate lump of the medical fluid to a resist longitudinal direction is conjectured that about several micrometers occur. Therefore, it is necessary to carry out the OPA lap of about 5 micrometers of the resist patterns to a circumference field, and to form them. Furthermore, in this operation form, the resist pattern 212 of the dot system which controls the rate of a throat area ratio of a circumference field, or a line system is formed in the circumference field 206.

[0045] Then, as shown in drawing 2 (c), specified quantity removal of the oxide film 210 exposed by the predetermined pattern by the boundary region 206 is carried out by the wet etching method. namely, the level difference after removal of an oxide film 210 -- datum level (abbreviation flat side of an effective element field), and abbreviation -- it carries out by controlling etching time so that it may become the same Although a thickness control [a little] more precise than the gestalt of the 1st operation is required in order to consider as **15 - 20% of level difference [at this time, for example, datum level,], especially a high controllability does not need. Moreover, since there are margins of enough also in a pattern size target, according to the wet etching method, a level difference is removable as a cheap method.

[0046] Thus, since a circumference level difference is removed and polish is completed so that the oxide film 210 of the circumference field 206 may not be removed completely, in the polish process by the CMP method, the circuit pattern density of the circumference field 206 acts as 0% of abbreviation.

[0047] Finally, as shown in drawing 2 (d), after removing the resist pattern 212, an oxide film 210 is ground by the CMP method. this time -- a ground level difference -- level difference datum level -- receiving -- abbreviation -- since it is the same, the maldistribution of the press force of a polish pad becomes small Therefore, it is prevented that polish speed is delayed, without the local polish speed difference occurring. Thus, since the polish speed of enough in an effective element field is in

equilibrium, the influence which it has on ****** of an effective element field is small. Therefore, since the circumference field where the level difference was removed does not affect the circuit pattern of an effective element field, it can acquire a good polish property in an effective element field.
[0048] this operation form -- **** -- if -- since the insulator layer of a circumference field is patternized so that it may become of the same grade as the circuit pattern density of an effective element field -- the polish property of a circumference field -- the polish property in an effective element field, and abbreviation -- it becomes the same Thus, although the ground circuit pattern density of a circumference field is 100% of abbreviation, since it is carrying out the predetermined patternizing of the insulator layer, it is served as 0% of circuit pattern densities. Moreover, since an actual circuit pattern is not processed like the conventional dummy element, the visibility of a marking field is not worsened. Moreover, since the level difference of the circuit pattern the non-formed field of a circumference field is canceled before CMP polish, productivity improves conventionally. Moreover, since it can respond with a mask common to all layers, the increase in the number of masks can be suppressed. Also about a mask design rule and a winning-by-taking-two-half-points way, since the precision of about several micrometers is enough, there are few mask manufactures and increases in cost on an aspect of practical use, and they end.
[0049] (Form of the 3rd operation) The manufacture method of the semiconductor device concerning the form of the 3rd operation is explained first, referring to drawing 3 . In addition, drawing 3 is cross-section process drawing for explaining the manufacture method of the semiconductor device concerning the form of the 3rd operation. In addition, the STI-CMP process is shown in this operation form. In addition, in this STI-CMP process, since the malfunction of a transistor element occurs when an oxide film remains on a nitride (active), it is important to ease the level difference of a circumference field.
[0050] First, as shown in drawing 3 (a), the insulator layer 310 which consists of an oxide film is formed on the semiconductor substrate 300 by which isolation structure (trench structure) is formed in the effective element field 302. At this time, the dummy element is not arranged in the circumference field 306. The maximum level difference of an oxide film 310 crosses to this circumference field 306 broadly, and is formed in it.
[0051] This operation form or the fundamental STI level difference structure of the semiconductor device to cut is the same as usual. Moreover, since a dummy element is not arranged to the circumference field 306, the circuit pattern density of the circumference field 306 became 100% of abbreviation, and the level difference of the oxide film 310 of the same grade as the trench depth has generated it.
[0052] Subsequently, as shown in drawing 3 (b), the resist pattern 312 for masking 306 in an effective element field and the G/L field 304 is deposited on an oxide film 310 by package exposure. It is desirable to form the resist pattern 312 at this time 306, for example, a 5-micrometer circumference field. This is the oxide-film removal process (for example, wet etching process) which is the following process, and is because a permeate lump of the medical fluid to a resist longitudinal direction is conjectured that about several micrometers occur. Therefore, it is necessary to carry out the OPA lap of about 5 micrometers of the resist patterns to a circumference field, and to form them.
[0053] Then, as shown in drawing 3 (c), the oxide film 310 exposed in the circumference field 306 is removed by the wet etching method. In this STI-CMP process, since there are few amounts of polishes of an oxide film, the oxide film which remains serves as a mask and removal of a nitride becomes difficult after polish ends the oxide film of a circumference field in the state where it remained, a resist mask removes the oxide film of a circumference field completely beforehand. Since a nitride 308 turns into [etch selectivity with the nitride 308 of a ground] a stopper film is easy to be obtained according to the wet etching method at this time, it is not necessary to control etching time in consideration of the level difference after removal of an oxide film 310. Therefore, since the need of the high controllability is not carried out but there are margins of enough also in a pattern size target, according to the wet etching method, a level difference is removable at an oxide-film removal process, as a cheap method.
[0054] Finally, as shown in drawing 3 (d), after removing the resist pattern 312, an oxide film 310 is ground by the CMP method. Since the level difference of the circumference field which is pattern a non-formed field is canceled before CMP polish at this time, the maldistribution of the press force of a polish pad becomes small, and it is prevented that polish speed is delayed in an effective element field. Consequently, since an oxide film does not remain in an effective element field, a semiconductor device can be operated normally.
[0055] In addition, since the front shell nitride 308 of CMP polish is exposed in the circumference field, although it is considered depending on the slurry (for example, slurry with the small polish selection ratio of the 310/nitrides 308 of oxide films, such as a KOH slurry) to be used that the nitride 308 to expose is also ground and the semiconductor substrate (for example, Si substrate) 300 of a ground is also exposed, an effective element field is hardly affected.
[0056] Since this operation form **** is not what processes an actual circuit pattern like the conventional dummy element, it does not worsen the visibility of a marking field. Since the level difference of the circuit pattern the non-formed field outside an effective element field is canceled before CMP polish, productivity improves conventionally. Moreover, since it can respond with a mask common to all layers, the increase in the number of masks can be suppressed. Also about a mask design rule and a winning-by-taking-two-half-points way, since the precision of about several micrometers is enough, there are few mask manufactures and increases in cost on an aspect of practical use, and they end.
[0057] (Form of the 4th operation) In this operation form, in order to make the polish property of a circumference field approximate with the polish property of an effective element field as compared with the form of the 3rd operation, a predetermined circuit pattern is formed in a circumference field.
[0058] First, the manufacture method of the semiconductor device concerning the form of the 4th operation is explained,

referring to drawing 4 . In addition, drawing 4 is cross-section process drawing for explaining the manufacture method of the semiconductor device concerning the form of the 4th operation. In addition, the STI-CMP process is shown in this operation form.

[0059] First, as shown in drawing 4 (a), the insulator layer 410 which consists of an oxide film is formed on the semiconductor substrate 400 by which isolation structure (trench structure) is formed in the effective element field 402. At this time, the dummy element is not arranged in the circumference field 406. The maximum level difference of an oxide film 410 crosses to this circumference field 406 broadly, and is formed in it.

[0060] This operation form or the fundamental STI level difference structure of the semiconductor device to cut is the same as usual. Moreover, since a dummy element is not arranged to the circumference field 406, the circuit pattern density of the circumference field 406 became 100% of abbreviation, and the level difference of the oxide film 410 of the same grade as the trench depth has generated it.

[0061] Subsequently, as shown in drawing 4 (b), the resist pattern 412 masked for masking 406 in an effective element field and the G/L field 404 by package exposure is deposited on an oxide film 410. It is desirable to form the resist pattern 412 at this time 406, for example, a 5-micrometer circumference field. This is the oxide-film removal process (for example, wet etching process) which is the following process, and is because a permeate lump of the medical fluid to a resist longitudinal direction is conjectured that about several micrometers occur. Therefore, it is necessary to carry out the OPA lap of about 5 micrometers of the resist patterns to a circumference field, and to form them. Furthermore, in this operation form, the resist pattern 412 of the dot system which controls the rate of a throat area ratio of a circumference field, or a line system is formed in the circumference field 406.

[0062] Then, as shown in drawing 4 (c), the oxide film 410 exposed by the predetermined pattern in the circumference field 406 is removed by the wet etching method. In this STI-CMP process, since there are few amounts of polishes of an oxide film, the oxide film which remains serves as a mask and removal of a nitride becomes difficult after polish ends the oxide film of a circumference field in the state where it remained, a resist mask removes beforehand the oxide film of the predetermined pattern exposed in a circumference field. Since a nitride 408 turns into [etch selectivity with the nitride 408 of a ground] a stopper film is easy to be obtained according to the wet etching method at this time, it is not necessary to control etching time in consideration of the level difference after removal of an oxide film 410. However, the lateral resist pattern float twisted for sinking in takes some cautions. Therefore, since the need of the high controllability is not carried out but there are margins of enough also in a pattern size target, according to the wet etching method, a level difference is removable at an oxide-film removal process, as a cheap method.

[0063] Finally, as shown in drawing 4 (d), after removing the resist pattern 412, an oxide film 410 is ground by the CMP method. Since the level difference of the circumference field which is pattern a non-formed field is canceled before CMP polish at this time, the maldistribution of the press force of a polish pad becomes small, and it is prevented that polish speed is delayed in an effective element field. Consequently, since an oxide film does not remain in an effective element field, a semiconductor device can be operated normally.

[0064] In addition, since the level difference of a circumference field is controlled at this time, superfluous polish is suppressed and the semiconductor substrate (Si substrate) of a ground is not exposed.

[0065] this operation form -- **** -- if -- moreover, the visibility of ** which is not what processes an actual circuit pattern like the conventional dummy element, and a marking field is not worsened Since the level difference of the circuit pattern the non-formed field outside an effective element field is canceled before CMP polish, productivity improves conventionally. Moreover, since the predetermined pattern is formed in the oxide film of a circumference field, it is necessary to hardly take into consideration that Si substrate of the ground of a circumference field is exposed like the form of the 3rd operation. Moreover, since it can respond with a mask common to all layers, the increase in the number of masks can be suppressed. Also about a mask design rule and a winning-by-taking-two-half-points way, since the precision of about several micrometers is enough, there are few mask manufactures and increases in cost on an aspect of practical use, and they end.

[0066] As mentioned above, although the form of the suitable operation concerning this invention was explained, this invention is not limited to this composition. If it is this contractor, various kinds of examples of correction and examples of change can be assumed within the limits of the technical thought indicated by the claim, and it will be understood as what is included also about those examples of correction, and the example of change by the technical range of this invention.

[0067] For example, in this operation form, although the composition which removes an oxide film by the wet etching method was mentioned as the example and explained, other etching methods are also employable.

[0068]

[Effect of the Invention] In a CMP process, since the maldistribution of the press force of a polish pad becomes small, the difference of polish speed is eased and the influence of ****** on the insulator layer of an effective element field is avoided.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

TECHNICAL FIELD

[The technical field to which invention belongs] this invention relates to the manufacture method of the semiconductor device which includes in a detail the process which carries out flattening of the insulator layer with the level difference formed on the semiconductor substrate by the CMP method further about the manufacture method of a semiconductor device.
[0002]

[Translation done.]

TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] However, by the above-mentioned conventional method, there are the following problems, for example in the typical isolation (STI:Shallow Trench Isolation) CMP process which is a CMP adoption process, and the flattening (IMD/PMD:Inter Metal Dielectrics/Pre Metal Dielectrics) CMP process of the wiring level difference formed on the insulator layer.

[0019] (The 1st problem) Since it is necessary to perform patterning besides an effective element field in order to form a dummy element in a circumference field, the productivity (here, CoO (Cost Of Ownership) not only including a throughput but all production cost and man days is called productivity) in an exposure process falls remarkably. Moreover, although this patterning must be performed at all CMP processes, since it is not what contributes to productivity, there is a problem that mass-production nature gets worse.

[0020] (The 2nd problem) Although the marking field which carries out laser printing of the lot history (ID) exists in a circumference field again, in order to prevent visibility aggravation of a marking character, a dummy element is not arranged in this marking field. Thus, since the field in which a circuit pattern is not formed adjoins and exists in an effective element field, there is a problem that a polish property gets worse locally in a field in part.

[0021] Therefore, the purpose of this invention is in the thing which can acquire a suitable polish property and for which new and the improved manufacture method of a semiconductor device are offered in the flattening process by the CMP method, without reducing productivity.

[Translation done.]

MEANS

[Means for Solving the Problem] In order to solve the above-mentioned technical problem, in invention according to claim 1 An insulator layer with the level difference formed on the semiconductor substrate by the CMP method The process which forms an insulator layer all over the semiconductor substrate containing the effective element field in which it is the manufacture method of a semiconductor device including the process which carries out flattening, and the element composition member was formed, and the boundary region in which an element composition member is not formed, The process which forms a resist mask on the aforementioned insulator layer of the boundary region within predetermined distance from the aforementioned effective element field and the aforementioned effective element field, The manufacture method of the semiconductor device characterized by having the process which carries out specified quantity removal of the insulator layer exposed by the aforementioned boundary region by etching, the process which removes the aforementioned resist mask, and the process which carries out flattening of the aforementioned insulator layer by the CMP method is offered.
[0023] In invention given in this paragraph, since the maldistribution of the pressure of the polish pad in a CMP process becomes small, the difference of polish speed is eased and the influence of ****** on the oxide film in an effective element field is avoided. Moreover, since it is not necessary to actually process a circuit pattern like the conventional dummy element, productivity improves. Furthermore, degradation of the visibility of a marking field is prevented before and after a polish process and after the following process.
[0024] moreover, the aforementioned resist mask is formed in the boundary region within the distance of 5 micrometers of abbreviation from the aforementioned effective element field and the aforementioned effective element field at least like invention according to claim 2 -- it needs -- constituting is desirable At the oxide-film removal process (for example, wet etching process) which is the following process, it can consider as the design in consideration of the permeate lump of the medical fluid to a resist longitudinal direction.
[0025] moreover, the aforementioned resist mask is further formed also in the predetermined field of the aforementioned boundary region by the predetermined pattern like invention according to claim 3 -- it needs -- if constituted, since the level difference density of the oxide film of a boundary region will become of the same grade as the level difference density in an effective element field, the press force of a polish pad is also equalized Consequently, it is hard coming to generate the polish speed difference, and dispersion in residual membrane thickness is improved. Moreover, since it is not necessary to actually process a circuit pattern like the conventional dummy element, degradation of the visibility of a marking field is prevented before and after a polish process and after the following process.
[0026] In the process which carries out specified quantity removal of the insulator layer exposed by the aforementioned boundary region by etching like invention according to claim 4, moreover, the insulator layer exposed by the aforementioned boundary region it considers as the abbreviation flat part of an insulator layer and the thickness of abbreviation same height which were formed in the aforementioned effective element field -- it needs -- if constituted, since the level difference density of the oxide film of a boundary region will become of the same grade as the level difference density in an effective element field further, the press force of a polish pad is also equalized Consequently, further, it is hard coming to generate the polish speed difference, and dispersion in residual membrane thickness is improved.
[0027] moreover, the aforementioned element composition member is the wiring formed on the semiconductor substrate like invention according to claim 5 -- it needs -- if constituted, in case the level difference of the layer insulation film formed on wiring will be ground by the CMP method, a polish property improves
[0028] moreover, the aforementioned element composition member is an active region which has the isolation structure formed on the semiconductor substrate like invention according to claim 6 -- it needs -- if constituted, the polish property in the CMP flattening process of the oxide film in an isolation process will improve
[0029] moreover, on the semiconductor substrate which has the aforementioned isolation structure, the nitride is formed like invention according to claim 7, and the aforementioned nitride functions as a stopper film of etching in the process which carries out specified quantity removal of the insulator layer exposed by the aforementioned boundary region by etching -- it needs -- if constituted, in the process which removes an insulator layer, it is not necessary to carry out time control of the level difference formed strictly
[0030] moreover, in the process which carries out specified quantity removal of the insulator layer exposed by the aforementioned boundary region by etching like invention according to claim 8, the aforementioned etching is performed by the wet etching method -- it needs -- if constituted, an oxide film is removable by the cheap method

[0031]
[Embodiments of the Invention] Hereafter, the gestalt of suitable operation of this invention is explained in detail, referring to an accompanying drawing. In addition, in the following explanation and an accompanying drawing, duplication explanation is omitted by ****** which attaches the same sign about the component which has the same function and same composition.
[0032] (Gestalt of the 1st operation) The manufacture method of the semiconductor device concerning the gestalt of the 1st operation is explained first, referring to drawing 1 . In addition, drawing 1 is cross-section process drawing for explaining the manufacture method of the semiconductor device concerning the gestalt of the 1st operation. In addition, the IMD/PMD-CMP process is shown in this operation gestalt.
[0033] First, as shown in drawing 1 (a), the insulator layer 110 which consists of an oxide film is formed on the semiconductor substrate 100 by which wiring 108 is formed in the effective element field 102. At this time, the dummy element is not arranged at a boundary region 106. The maximum level difference of an oxide film 110 includes this boundary region 106 broadly, and is formed in it.
[0034] This operation gestalt or the fundamental wiring level difference structure of the semiconductor device to cut is the same as usual. Moreover, since a dummy element is not arranged to a boundary region 106, the circuit pattern density of a boundary region 106 is 100% of abbreviation, and the level difference of the oxide film 110 of the same grade as wiring height has generated it.
[0035] Subsequently, as shown in drawing 1 (b), the resist pattern 112 for masking 102 in an effective element field and the G/L field 104 is deposited on an oxide film 110 by package exposure. It is desirable to form the resist pattern 112 at this time 106, for example, a 5-micrometer circumference field. Since this is equal to the height of a wiring level difference as an amount of removal of an oxide film, it is the oxide-film removal process (for example, wet etching process) which is the following process, and is because a permeate lump of the medical fluid to a resist longitudinal direction is conjectured that about several micrometers occur. Therefore, it is necessary to carry out the OPA lap of about 5 micrometers of the resist patterns to a boundary region, and to form them.
[0036] Then, as shown in drawing 1 (c), specified quantity removal of the oxide film 110 exposed by the boundary region 106 is carried out by the wet etching method. namely, the level difference after removal of an oxide film 110 -- datum level (abbreviation flat side of an effective element field), and abbreviation -- it carries out by controlling etching time so that it may become the same However, it is not necessary to perform a precise thickness control, and it is sufficient if it controls to the grade which wiring 108 does not expose. Therefore, since the need of the high controllability is not carried out but there are margins of enough also in a pattern size target, according to the wet etching method, a level difference is removable at an oxide-film removal process, as a cheap method.
[0037] Thus, since a circumference level difference is removed and polish is completed so that the oxide film 110 of a boundary region 106 may not be removed completely, in the polish process by the CMP method, the circuit pattern density of a boundary region 106 acts as 0% of abbreviation.
[0038] Finally, as shown in drawing 1 (d), after removing the resist pattern 112, an oxide film 110 is ground by the CMP method. this time -- a ground level difference -- level difference datum level -- receiving -- abbreviation -- since it is the same, the maldistribution of the press force of a polish pad becomes small Therefore, it is prevented that polish speed is delayed in an effective element field, without the polish speed difference occurring locally. Thus, since the polish speed of enough in an effective element field is in equilibrium, the influence which it has on ****** of an effective element field is small. Therefore, since the boundary region from which the level difference was removed does not affect the circuit pattern of an effective element field, it can acquire a good polish property in an effective element field.
[0039] Although ground circuit pattern density is 100% of abbreviation, since this operation gestalt **** has removed the level difference of a boundary region, it serves it as 0% of circuit pattern densities in a CMP process. Moreover, since an actual circuit pattern is not processed like the conventional dummy element, the visibility of a marking field is not worsened. Since the level difference of the pattern the non-formed field outside an effective element field is canceled before CMP polish, productivity improves conventionally. Moreover, since it can respond with a mask common to all layers, the increase in the number of masks can be suppressed. Also about a mask design rule and a winning-by-taking-two-half-points way, since the precision of about several micrometers is enough, there are few mask manufactures and increases in cost on an aspect of practical use, and they end.
[0040] (Gestalt of the 2nd operation) In this operation gestalt, in order to make the polish property of a boundary region approximate with the polish property of an effective element field as compared with the gestalt of the 1st operation, a predetermined circuit pattern is formed in a boundary region.
[0041] First, the manufacture method of the semiconductor device concerning the gestalt of the 2nd operation is explained, referring to drawing 2 . In addition, drawing 2 is cross-section process drawing for explaining the manufacture method of the semiconductor device concerning the gestalt of the 2nd operation. In addition, the IMD/PMD-CMP process is shown in this operation gestalt.
[0042] First, as shown in drawing 2 (a), the insulator layer 210 which consists of an oxide film is formed on the semiconductor substrate 200 by which wiring 208 is formed in the effective element field 202. At this time, the dummy element is not arranged at a boundary region 206. The maximum level difference of an oxide film 210 includes this boundary region 206 broadly, and is formed in it.
[0043] This operation gestalt or the fundamental wiring level difference structure of the semiconductor device to cut is the

same as usual. Moreover, since a dummy element is not arranged to a boundary region 206, the circuit pattern density of a boundary region 206 is 100% of abbreviation, and the level difference of the oxide film 210 of the same grade as wiring height has generated it.
[0044] Subsequently, as shown in drawing 2 (b), the resist pattern 212 for masking 202 in an effective element field and the G/L field 204 is deposited on an oxide film 210 by package exposure. It is desirable to form the resist pattern 212 at this time 206, for example, a 5-micrometer circumference field. Since this is equal to the height of a wiring level difference as an amount of removal of an oxide film, it is the oxide-film removal process (for example, wet etching process) which is the following process, and is because a permeate lump of the medical fluid to a resist longitudinal direction is conjectured that about several micrometers occur. Therefore, it is necessary to carry out the OPA lap of about 5 micrometers of the resist patterns to a boundary region, and to form them. Furthermore, in this operation gestalt, the resist pattern 212 of the dot system which controls the rate of a throat area ratio of a boundary region, or a line system is formed in a boundary region 206.
[0045] Then, as shown in drawing 2 (c), specified quantity removal of the oxide film 210 exposed by the predetermined pattern by the boundary region 206 is carried out by the wet etching method. namely, the level difference after removal of an oxide film 210 -- datum level (abbreviation flat side of an effective element field), and abbreviation -- it carries out by controlling etching time so that it may become the same Although a thickness control [a little] more precise than the gestalt of the 1st operation is required in order to consider as **15 - 20% of level difference [at this time, for example, datum level,], especially a high controllability does not need. Moreover, since there are margins of enough also in a pattern size target, according to the wet etching method, a level difference is removable as a cheap method.
[0046] Thus, since a circumference level difference is removed and polish is completed so that the oxide film 210 of a boundary region 206 may not be removed completely, in the polish process by the CMP method, the circuit pattern density of a boundary region 206 acts as 0% of abbreviation.
[0047] Finally, as shown in drawing 2 (d), after removing the resist pattern 212, an oxide film 210 is ground by the CMP method. this time -- a ground level difference -- level difference datum level -- receiving -- abbreviation -- since it is the same, the maldistribution of the press force of a polish pad becomes small Therefore, it is prevented that polish speed is delayed, without the local polish speed difference occurring. Thus, since the polish speed of enough in an effective element field is in equilibrium, the influence which it has on ****** of an effective element field is small. Therefore, since the boundary region from which the level difference was removed does not affect the circuit pattern of an effective element field, it can acquire a good polish property in an effective element field.
[0048] this operation gestalt -- **** -- if -- since the insulator layer of a boundary region is patternized so that it may become of the same grade as the circuit pattern density of an effective element field -- the polish property of a boundary region -- the polish property in an effective element field, and abbreviation -- it becomes the same Thus, although the ground circuit pattern density of a boundary region is 100% of abbreviation, since it is carrying out the predetermined patternizing of the insulator layer, it is served as 0% of circuit pattern densities. Moreover, since an actual circuit pattern is not processed like the conventional dummy element, the visibility of a marking field is not worsened. Moreover, since the level difference of the circuit pattern the non-formed field of a boundary region is canceled before CMP polish, productivity improves conventionally. Moreover, since it can respond with a mask common to all layers, the increase in the number of masks can be suppressed. Also about a mask design rule and a winning-by-taking-two-half-points way, since the precision of about several micrometers is enough, there are few mask manufactures and increases in cost on an aspect of practical use, and they end.
[0049] (Gestalt of the 3rd operation) The manufacture method of the semiconductor device concerning the gestalt of the 3rd operation is explained first, referring to drawing 3 . In addition, drawing 3 is cross-section process drawing for explaining the manufacture method of the semiconductor device concerning the gestalt of the 3rd operation. In addition, the STI-CMP process is shown in this operation gestalt. In addition, in this STI-CMP process, since the malfunction of a transistor element occurs when an oxide film remains on a nitride (active), it is important to ease the level difference of a boundary region.
[0050] First, as shown in drawing 3 (a), the insulator layer 310 which consists of an oxide film is formed on the semiconductor substrate 300 by which isolation structure (trench structure) is formed in the effective element field 302. At this time, the dummy element is not arranged at a boundary region 306. The maximum level difference of an oxide film 310 includes this boundary region 306 broadly, and is formed in it.
[0051] This operation form or the fundamental STI level difference structure of the semiconductor device to cut is the same as usual. Moreover, since a dummy element is not arranged to the circumference field 306, the circuit pattern density of the circumference field 306 became 100% of abbreviation, and the level difference of the oxide film 310 of the same grade as the trench depth has generated it.
[0052] Subsequently, as shown in drawing 3 (b), the resist pattern 312 for masking 306 in an effective element field and the G/L field 304 is deposited on an oxide film 310 by package exposure. It is desirable to form the resist pattern 312 at this time 306, for example, a 5-micrometer circumference field. This is the oxide-film removal process (for example, wet etching process) which is the following process, and is because a permeate lump of the medical fluid to a resist longitudinal direction is conjectured that about several micrometers occur. Therefore, it is necessary to carry out the OPA lap of about 5 micrometers of the resist patterns to a circumference field, and to form them.
[0053] Then, as shown in drawing 3 (c), the oxide film 310 exposed in the circumference field 306 is removed by the wet etching method. In this STI-CMP process, since there are few amounts of polishes of an oxide film, the oxide film which remains serves as a mask and removal of a nitride becomes difficult after polish ends the oxide film of a circumference field

in the state where it remained, a resist mask removes the oxide film of a circumference field completely beforehand. Since a nitride 308 turns into [etch selectivity with the nitride 308 of a ground] a stopper film is easy to be obtained according to the wet etching method at this time, it is not necessary to control etching time in consideration of the level difference after removal of an oxide film 310. Therefore, since the need of the high controllability is not carried out but there are margins of enough also in a pattern size target, according to the wet etching method, a level difference is removable at an oxide-film removal process, as a cheap method.

[0054] Finally, as shown in drawing 3 (d), after removing the resist pattern 312, an oxide film 310 is ground by the CMP method. Since the level difference of the boundary region which is pattern a non-formed field is canceled before CMP polish at this time, the maldistribution of the press force of a polish pad becomes small, and it is prevented that polish speed is delayed in an effective element field. Consequently, since an oxide film does not remain in an effective element field, a semiconductor device can be operated normally.

[0055] In addition, since the front shell nitride 308 of CMP polish is exposed in the boundary region, although it is considered depending on the slurry (for example, slurry with the small polish selection ratio of the 310/nitrides 308 of oxide films, such as a KOH slurry) to be used that the nitride 308 to expose is also ground and the semiconductor substrate (for example, Si substrate) 300 of a ground is also exposed, an effective element field is hardly affected.

[0056] Since this operation gestalt **** is not what processes an actual circuit pattern like the conventional dummy element, it does not worsen the visibility of a marking field. Since the level difference of the circuit pattern the non-formed field outside an effective element field is canceled before CMP polish, productivity improves conventionally. Moreover, since it can respond with a mask common to all layers, the increase in the number of masks can be suppressed. Also about a mask design rule and a winning-by-taking-two-half-points way, since the precision of about several micrometers is enough, there are few mask manufactures and increases in cost on an aspect of practical use, and they end.

[0057] (Gestalt of the 4th operation) In this operation gestalt, in order to make the polish property of a boundary region approximate with the polish property of an effective element field as compared with the gestalt of the 3rd operation, a predetermined circuit pattern is formed in a boundary region.

[0058] First, the manufacture method of the semiconductor device concerning the gestalt of the 4th operation is explained, referring to drawing 4 . In addition, drawing 4 is cross-section process drawing for explaining the manufacture method of the semiconductor device concerning the gestalt of the 4th operation. In addition, the STI-CMP process is shown in this operation gestalt.

[0059] First, as shown in drawing 4 (a), the insulator layer 410 which consists of an oxide film is formed on the semiconductor substrate 400 by which isolation structure (trench structure) is formed in the effective element field 402. At this time, the dummy element is not arranged at a boundary region 406. The maximum level difference of an oxide film 410 includes this boundary region 406 broadly, and is formed in it.

[0060] This operation gestalt or the fundamental STI level difference structure of the semiconductor device to cut is the same as usual. Moreover, since a dummy element is not arranged to a boundary region 406, the circuit pattern density of a boundary region 406 became 100% of abbreviation, and the level difference of the oxide film 410 of the same grade as the trench depth has generated it.

[0061] Subsequently, as shown in drawing 4 (b), the resist pattern 412 masked for masking 406 in an effective element field and the G/L field 404 by package exposure is deposited on an oxide film 410. It is desirable to form the resist pattern 412 at this time 406, for example, a 5-micrometer circumference field. This is the oxide-film removal process (for example, wet etching process) which is the following process, and is because a permeate lump of the medical fluid to a resist longitudinal direction is conjectured that about several micrometers occur. Therefore, it is necessary to carry out the OPA lap of about 5 micrometers of the resist patterns to a boundary region, and to form them. Furthermore, in this operation gestalt, the resist pattern 412 of the dot system which controls the rate of a throat area ratio of a boundary region, or a line system is formed in a boundary region 406.

[0062] Then, as shown in drawing 4 (c), the oxide film 410 exposed by the predetermined pattern by the boundary region 406 is removed by the wet etching method. In this STI-CMP process, since there are few amounts of polishes of an oxide film, the oxide film which remains serves as a mask and removal of a nitride becomes difficult after polish ends the oxide film of a boundary region in the state where it remained, a resist mask removes beforehand the oxide film of the predetermined pattern exposed by the boundary region. Since a nitride 408 turns into [etch selectivity with the nitride 408 of a ground] a stopper film is easy to be obtained according to the wet etching method at this time, it is not necessary to control etching time in consideration of the level difference after removal of an oxide film 410. However, the lateral resist pattern float twisted for sinking in takes some cautions. Therefore, since the need of the high controllability is not carried out but there are margins of enough also in a pattern size target, according to the wet etching method, a level difference is removable at an oxide-film removal process, as a cheap method.

[0063] Finally, as shown in drawing 4 (d), after removing the resist pattern 412, an oxide film 410 is ground by the CMP method. Since the level difference of the boundary region which is pattern a non-formed field is canceled before CMP polish at this time, the maldistribution of the press force of a polish pad becomes small, and it is prevented that polish speed is delayed in an effective element field. Consequently, since an oxide film does not remain in an effective element field, a semiconductor device can be operated normally.

[0064] In addition, since the level difference of a boundary region is controlled at this time, superfluous polish is suppressed

and the semiconductor substrate (Si substrate) of a ground is not exposed.
[0065] this operation gestalt -- **** -- if -- moreover, the visibility of ** which is not what processes an actual circuit pattern like the conventional dummy element, and a marking field is not worsened Since the level difference of the circuit pattern the non-formed field outside an effective element field is canceled before CMP polish, productivity improves conventionally. Moreover, since the predetermined pattern is formed in the oxide film of a boundary region, it is necessary to hardly take into consideration that Si substrate of the ground of a boundary region is exposed like the gestalt of the 3rd operation. Moreover, since it can respond with a mask common to all layers, the increase in the number of masks can be suppressed. Also about a mask design rule and a winning-by-taking-two-half-points way, since the precision of about several micrometers is enough, there are few mask manufactures and increases in cost on an aspect of practical use, and they end.
[0066] As mentioned above, although the gestalt of the suitable operation concerning this invention was explained, this invention is not limited to this composition. If it is this contractor, various kinds of examples of correction and examples of change can be assumed within the limits of the technical thought indicated by the claim, and it will be understood as what is included also about those examples of correction, and the example of change by the technical range of this invention.
[0067] For example, in this operation gestalt, although the composition which removes an oxide film by the wet etching method was mentioned as the example and explained, other etching methods are also employable.

[Translation done.]

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is cross-section process drawing showing the manufacture method of the semiconductor device concerning the gestalt of the 1st operation.
[Drawing 2] It is cross-section process drawing showing the manufacture method of the semiconductor device concerning the gestalt of the 2nd operation.
[Drawing 3] It is cross-section process drawing showing the manufacture method of the semiconductor device concerning the gestalt of the 3rd operation.
[Drawing 4] It is cross-section process drawing showing the manufacture method of the semiconductor device concerning the gestalt of the 4th operation.
[Drawing 5] It is cross-section process drawing showing the semiconductor device in the former.
[Drawing 6] It is cross-section process drawing showing the semiconductor device in the former.
[Drawing 7] It is cross-section process drawing showing the manufacture method of the semiconductor device which can be set conventionally.
[Drawing 8] It is cross-section process drawing showing the manufacture method of a semiconductor device that the former can be set.
[Description of Notations]
100 Semiconductor Substrate
102 Effective Chip Field
104 Grid Line (G/L) Field
106 Boundary Region
108 Wiring
110 Oxide Film
112 Resist
114 Polish Pad

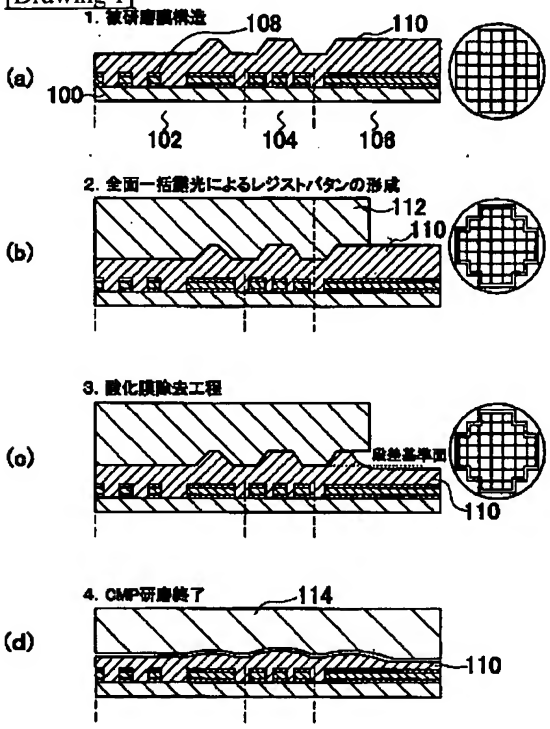
[Translation done.]

* NOTICES *

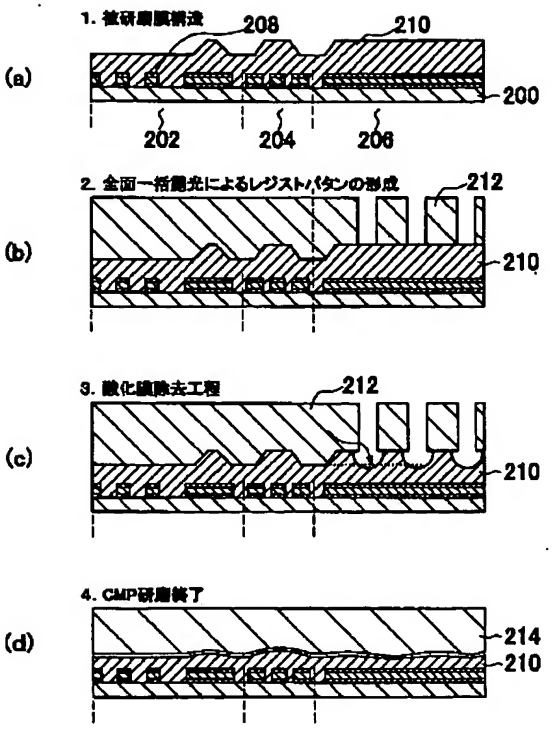
1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

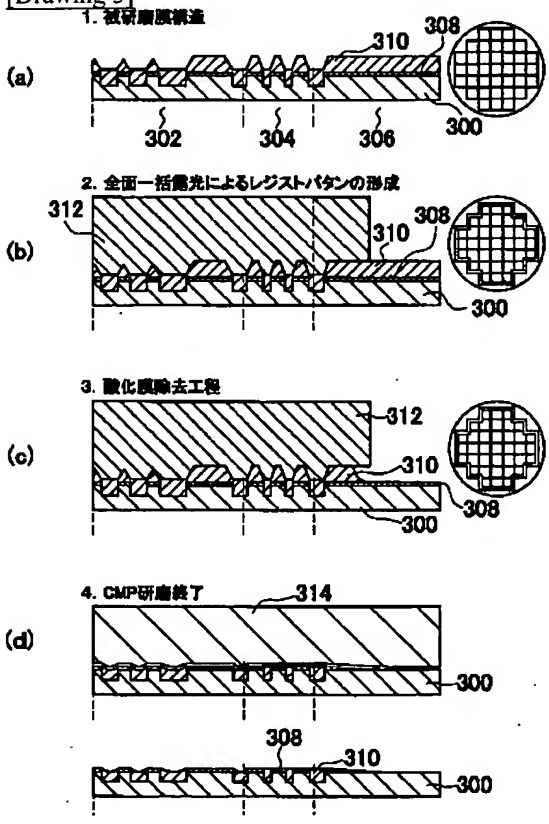
[Drawing 1]



[Drawing 2]



[Drawing 3]



[Drawing 4]

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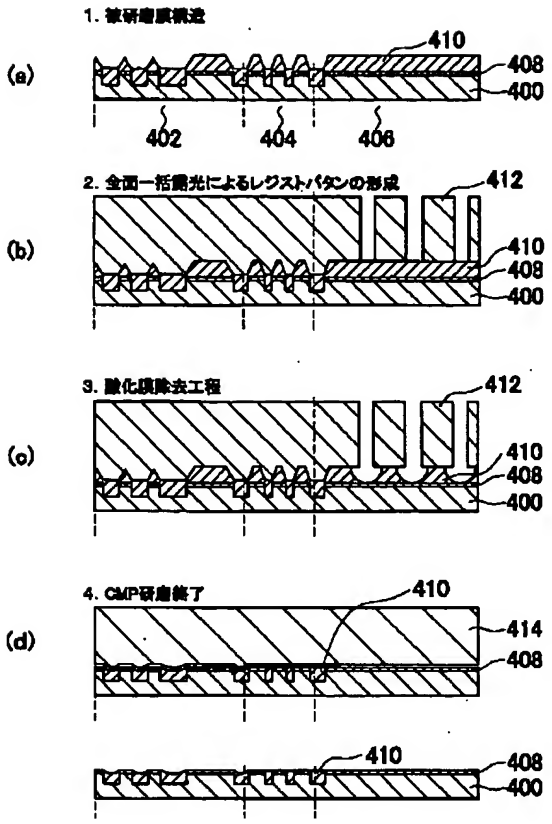
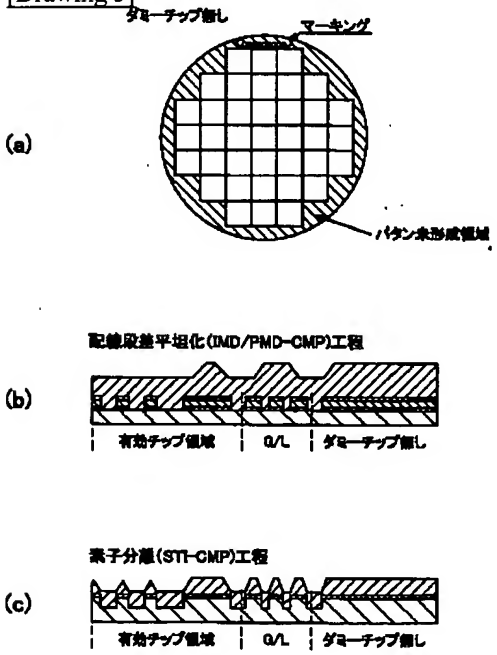


[Drawing 5]



[Drawing 6]

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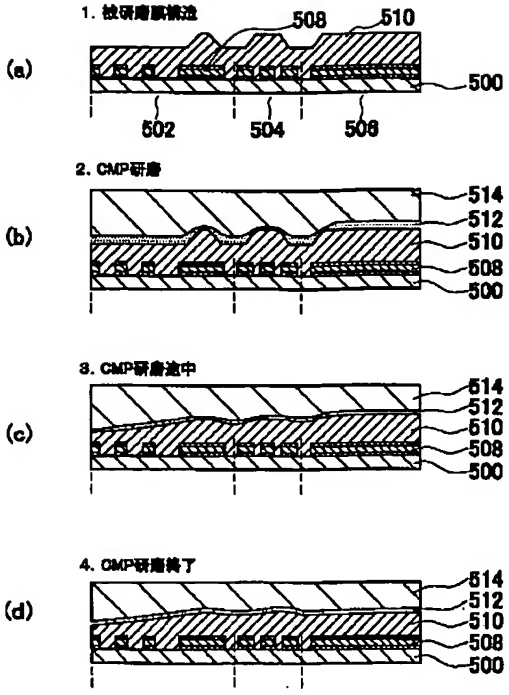
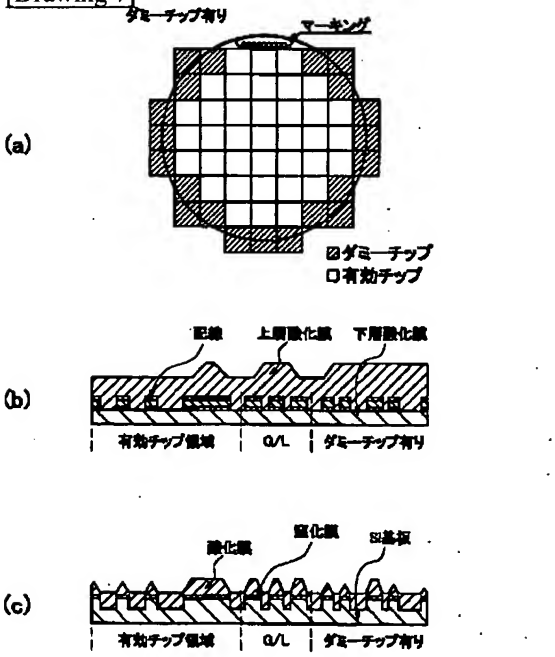


[Drawing 7]



[Drawing 8]

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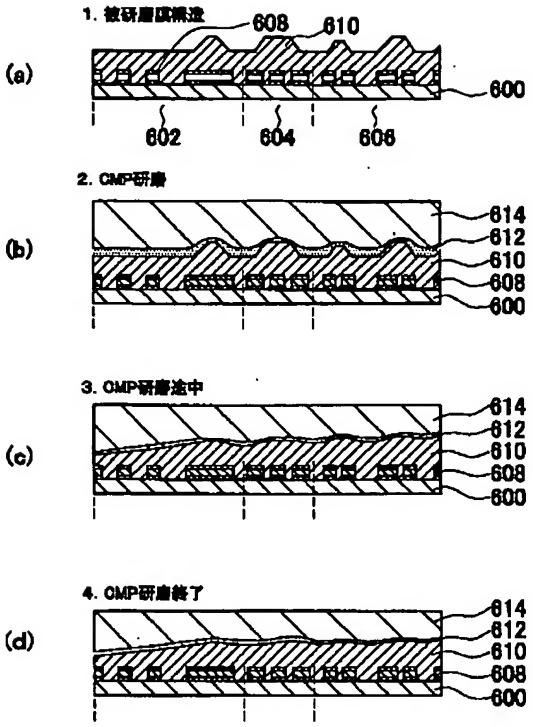

[Translation done.]